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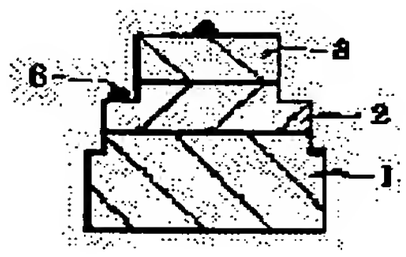
(54) MANUFACTURE OF GALLIUM NITRIDE SERIES COMPOUND SEMICONDUCTOR CHIP

(57)Abstract:
PURPOSE: To separate a sapphire board into chip states without impairing crystallizability of gallium nitride series semiconductor laminated on a board by cutting the board by dicing or scribing.
CONSTITUTION: A protective layer is first provided on a p-type layer 3 of an uppermost layer of a wafer laminated on a sapphire board 1. The layer 3 is etched up to an n-type layer 2. After the etching is finished, the protective layer is removed. Further, the layer 2 is etched or diced to the board 1 except a space provided with an n-type electrode on a surface of the layer 2. Then, the board 1 is separated by dicing or scribing. The drawing shows a state in which electrodes 6 are formed on the separated layers 2, 3 of a gallium nitride series compound semiconductor element. Thus, a boundary between the layers 2 and 3, i.e., a p-n junction surface can be separated without stress.



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CLAIMS

[Claim(s)]
[Claim 1] The manufacture approach of the gallium-nitride system compound semiconductor chip which is the approach of separating the wafer with which the laminating of the gallium-nitride system compound semiconductor of n mold and p mold was carried out to order on silicon on sapphire in the shape of a chip, and is characterized by to provide the process which grinds silicon on sapphire and makes thin, the process which etch a part of p type layer to n type layer, and the process which cut etching or the process which carries out dicing, and silicon on sapphire for n type layer by dicing or scribing to silicon on sapphire.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the manufacture approach of the gallium nitride system compound semiconductor chip used for luminescence devices, such as a blue light emitting diode and a blue laser diode, and it relates to the approach of separating in the shape of a chip, without spoiling the crystallinity of the gallium nitride system compound semiconductor by which the laminating was especially carried out on silicon on sapphire.
[0002]
[Description of the Prior Art] Generally as for luminescence devices, such as a light emitting diode and a laser diode, the semiconductor chip which is a source of luminescence is installed on the stem. GaAs, GaAlAs, GaP, etc. are known for red, orange, yellow, and green light emitting diode as an ingredient which constitutes the semiconductor chip. Although many semiconductor materials are studied about blue diode and blue laser diode, it is still the experimental stage and has not resulted in utilization. However, gallium nitride system compound semiconductors, such as GaN, InGaN, and GaAlN, attract attention as a practical blue luminescent material.
[0003] Conventionally, generally as an approach of dividing into a chip the wafer with which the laminating of the semiconductor material was carried out, the dicer or the scriber is used. After a dicer carries out full cutting of the wafer or cuts the slot of width larger than edge-of-a-blade width deeply in rotation of the disk which is also usually called a dicing saw and uses the edge of a blade as a diamond, it is equipment cut according to external force. a both-way rectilinear motion of the needle which uses a tip as a diamond with a scriber on the other hand -- a scribe line (marking line) very thin to a wafer -- for example, after lengthening in a grid pattern, it is equipment cut according to external force.
[0004]
[Problem(s) to be Solved by the Invention] Since there is cleavage in the "110" directions, using this property, the crystal of zinc structure which does not carry said GaP, GaAs, etc. is a scriber, and can be separated easily [the shape of a chip] by putting in a scribe line in this direction. however, the so-called hetero-epi structure by which the laminating of the gallium nitride system compound semiconductor is carried out on silicon on sapphire -- it is -- a gallium nitride system compound semiconductor and sapphire -- lattice constant irregular ** -- it is large. Furthermore, sapphire does not have cleavage on the property of a crystal called hexagonal system. Therefore, having cut with a scriber was impossible. Moreover, since Mohs hardness was about 9 and the very hard matter, when full cutting of sapphire and the gallium nitride system compound semiconductor was carried out by the dicer, it becomes easy to generate a crack and a chipping in the cutting plane, and they were not able to be finely cut to it. Furthermore, when the cutting edge of a dicer touches a wafer cutting plane for a long time, stress (stress) arises in the longitudinal direction of a wafer. For this reason, since it became easy to generate a crack, a chipping, etc. in the interface of n type layer and p type layer and the crystallinity of an important gallium nitride system compound semiconductor was spoiled especially, there was a trouble that brightness will fall or a life will become very short.
[0005] Therefore, this invention is faced cutting the gallium nitride system compound semiconductor wafer which uses sapphire as a substrate in the shape of a chip, and the crack of a cutting plane and an interface and generating of a chipping are prevented, and while obtaining the gallium nitride system compound semiconductor chip which has the luminescence engine performance which was excellent, without spoiling the crystallinity of a gallium nitride system compound semiconductor, it aims at offering the approach of cutting with a sufficient yield in a desired form and size.
[0006]
[Means for Solving the Problem] The manufacture approach of the gallium nitride system compound semiconductor chip of this invention The process which is the approach of separating the wafer with which the laminating of the gallium nitride system compound semiconductor of n mold and p mold was carried out to order on silicon on sapphire in the shape of a chip, grinds ** silicon on sapphire, and is made thin, ** It is characterized by providing the process which etches a part of p type layer to n type layer, and the process which cuts etching or the process which carries out dicing, and ** silicon on sapphire for **n type layer by dicing or scribing to silicon on sapphire.
[0007] Hereafter, the manufacture approach of one example of this invention is explained in full detail, referring to a drawing. Drawing 1 - drawing 6 are a gallium nitride system compound semiconductor wafer and the sectional view showing the structure of a component, and, as for silicon on sapphire and 2, 1 is [n mold gallium nitride system compound semiconductor layer (henceforth n type layer) and 3] p mold gallium nitride system compound semiconductor layers (henceforth p type layer). However, the approach of this invention is not applied only to the gallium nitride system compound semiconductor wafer of the structure of a drawing.
[0008] Usually, the thickness of n type layer 2 by which the laminating of the thickness of a gallium nitride system compound semiconductor wafer was carried out 400-800 micrometers and on it by silicon on sapphire 1, and p type layer 3 is at most about ten micrometers, and the most is occupied by the thickness of silicon on sapphire 1. Therefore, in the process of **, it is desirable to grind silicon on sapphire 1 and to adjust the thickness to 50-300 micrometers. When thinner than 50 micrometers, it becomes and is in the inclination which curvature produces to a wafer that the whole wafer tends to break. Moreover, if thicker than 300 micrometers, in the process of **, it will become easy to generate a chipping and a crack in silicon on sapphire in the case of cutting by dicing or scribing. Moreover, when carrying out scribing, in order to

have to make a scribe line deep, there is an inclination for a fine chip to become impossible easily and for chip separation to become difficult. As still more desirable thickness of the ground substrate, it is 100-200 micrometers. In addition, the process of ** may be performed after the process of ** and **.

[0009] First, on silicon on sapphire 1, on p type layer 3 n type layer 2 and whose p type layer 3 are the maximum upper layers of the wafer by which the laminating was carried out to order, as shown in drawing 1 , a protective coat 4 is formed. After it prepares a protective coat 4 in order to perform pattern etching and it carries out patterning by the photoresist while it prevents p type layer 3 being eaten away by etching, it can be formed using a plasma-CVD method with the ingredient of SiO2 grade. In addition, in this drawing, silicon on sapphire 1 is ground beforehand and made thin.

[0010] Next, p type layer 3 in which the protective coat 4 was formed is etched to n type layer 2 (process of **). the etching approach -- dry cleaning -- wet -- which approach may be used. As shown in drawing 2 after etching termination, an acid removes a protective coat 4.

[0011] furthermore, the tooth space which can prepare n mold electrode in the front face of n type layer 2 as shown in drawing 3 -- leaving -- n type layer 2 -- up to silicon on sapphire 1 -- etching -- or dicing is carried out (process of **). Etching is desirable in order to make it not apply stress to the interface of n type layer 2 and silicon on sapphire 1 as much as possible. To etch, as mentioned above, it is necessary to form a protective coat in addition to an etching side (electrode formation parts of p type layer 3 and n type layer 2).

[0012] Next, as shown in drawing 4 , after carrying out scribing of the silicon on sapphire exposed according to the process of ** and putting in the scribe line (marking line) 5, a push rate is separated from a silicon-on-sapphire side (process of **). ** Since thickness of silicon on sapphire is made thin according to the process, it is finely separable in the shape of a chip by putting in, pushing and breaking the scribe line 5. Although especially the depth of a scribe line is not specified, by putting in in 5% or more of depth of the thickness of a substrate, sapphire without cleavage can also make a cutting plane a plane mostly, and can be cut preferably.

[0013] Moreover, as shown in drawing 5 , direct full cutting of the silicon on sapphire 1 may be carried out by dicing. Also in this case, since silicon on sapphire 1 is beforehand made thin, dicing time amount can be shortened, and it can cut finely, without applying stress.

[0014]

[Function] Drawing 6 is the sectional view showing the condition of having formed the electrode 6 in n type layer 2 and p type layer 3 of the gallium nitride system compound semiconductor element separated by scribing or the dicing of a process of **.

[0015] In this drawing, since the interface of n type layer 2 and p type layer 3, i.e., a p-n junction side, is etched, the stress by the conventional dicing does not start this interface, and most damages on a gallium nitride system compound semiconductor crystal cannot be found. Furthermore, also in the interface of silicon on sapphire 1 and n type layer 2, beforehand, according to the process of **, since the cutting depth can be shortened even if it performs dicing, since it is etched to the middle of n type layer 2, the rate which stress requires decreases sharply as compared with the former. Therefore, the crack of the gallium nitride system compound semiconductor layer to which the gallium nitride system compound semiconductor chip obtained by the approach of this invention originates in grid mismatching, and the chipping are prevented, and crystallinity is held, without damaging a semiconducting crystal. Moreover, by grinding silicon on sapphire and making it thin, silicon on sapphire without cleavage can also be finely cut by the scribe, and there is an outstanding advantage that cutting time amount can be shortened also in dicing.

[0016]

[Example] Hereafter, an example explains the manufacture approach of the gallium nitride system compound semiconductor chip of this invention.

[0017] A pattern is formed by the photoresist at the p mold GaN layer of the GaN epitaxial wafer for light emitting diodes into which the n mold GaN layer and the p mold GaN layer were grown up by the thickness of 5 micrometers in all in order on the silicon on sapphire of 450 micrometers in [example 1] thickness, and magnitude [of 2 inches] phi.

[0018] After forming SiO2 film by 0.1-micrometer thickness as a protective coat by the plasma-CVD method from on a photoresist, a photoresist is exfoliated with a solvent and it leaves SiO2 film by which patterning was carried out.

[0019] A wafer is immersed in the mixed acid of a phosphoric acid and a sulfuric acid, and a p mold GaN layer is etched to an n mold GaN layer.

[0020] Silicon on sapphire is ground to 150 micrometers with a grinder after etching.

[0021] A wafer is installed in a dicing saw after polish, and the dicing of the predetermined cutline (350-micrometer angle) top is carried out in a depth of 20 micrometers in a diamond blade on condition that blade engine-speed 30,000rpm and cutting speed 0.3 mm/sec.

[0022] Next, adhesive tape is stuck on a substrate side, and it sticks on the table of a scriber, and fixes by the vacuum chuck. A table moves to a x axis (right and left) and the y-axis (before or after), and has pivotable structure 180 degrees at the horizontal. After immobilization, the scribe of the marks of dicing is carried out with the diamond cutting edge of a scriber, and Rhine is lengthened. The bar with which the diamond cutting edge was formed has structure movable in the z-axis (upper and lower sides) and the direction of the y-axis (before or after). In order that the load to the edge of a blade of a diamond cutting edge may set to 100g and may make the depth of a scribe line deep, it is taken as a depth of 10 micrometers by carrying out the scribe of the same Rhine twice.

[0023] The GaN wafer which lengthened the scribe line was removed from the table, and the GaN chip was obtained by applying a pressure with a roller, pushing and dividing from a silicon-on-sapphire side.

[0024] Thus, when what is depended on a poor appearance from the obtained GaN chip was removed, the yield was 95% or more. Moreover, after attaching Au electrode in the p mold GaN layer of this GaN chip, and an n mold GaN layer, when it considered as light emitting diode according to the conventional method, in forward voltage 4.0V, the radiant power output was 50 microwatts and the luminescence life was 5000 hours or more.

[0025] After etching similarly the same GaN epitaxial wafer as the [example 1 of comparison] example 1 to an n mold GaN layer, when full cutting was similarly carried out to the chip of 350-micrometer angle on condition that blade engine-speed 30,000rpm and cutting speed 0.3 mm/sec using the direct dicer, without grinding silicon on sapphire, the countless crack

arose to the cutting plane line, and the yield was 30% or less. Moreover, when Au electrode was attached as well as p type layer and n type layer of a GaN chip which remained and having been considered as light emitting diode, in forward voltage 4.0V, 20 microwatts of radiant power outputs and a luminescence life were 50 - 70 hours.

[0026]

[Effect of the Invention] As stated above, according to the approach of this invention, the pn junction section is separable without stress, and the extensive improvement was accepted in property degradation which had become a problem conventionally especially the luminescence life, and the radiant power output. moreover, the lattice constant of a gallium nitride system compound semiconductor and silicon on sapphire -- since irregular, the crack of the crystal face to produce, a chipping, etc. can be prevented, a gallium nitride system compound semiconductor chip can be manufactured with a sufficient yield, and the utility value on the industry is large.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view showing the structure of the gallium nitride system compound semiconductor wafer obtained in the process of one example of this invention.
[Drawing 2] The sectional view showing the structure of the gallium nitride system compound semiconductor wafer obtained in the process of one example of this invention.
[Drawing 3] The sectional view showing the structure of the gallium nitride system compound semiconductor wafer obtained in the process of one example of this invention.
[Drawing 4] The sectional view showing the structure of the gallium nitride system compound semiconductor wafer obtained in the process of one example of this invention.
[Drawing 5] The sectional view showing the structure of the gallium nitride system compound semiconductor wafer obtained in the process of one example of this invention.
[Drawing 6] The sectional view showing the structure of the gallium nitride system compound semiconductor chip obtained in the process of one example of this invention.
[Description of Notations]
1 ..... Silicon on sapphire
2 ..... n mold gallium nitride system compound semiconductor layer
3 ..... p mold gallium nitride system compound semiconductor layer
4 ..... Protective coat
5 ..... Scribe line
6 ..... Electrode

[Translation done.]

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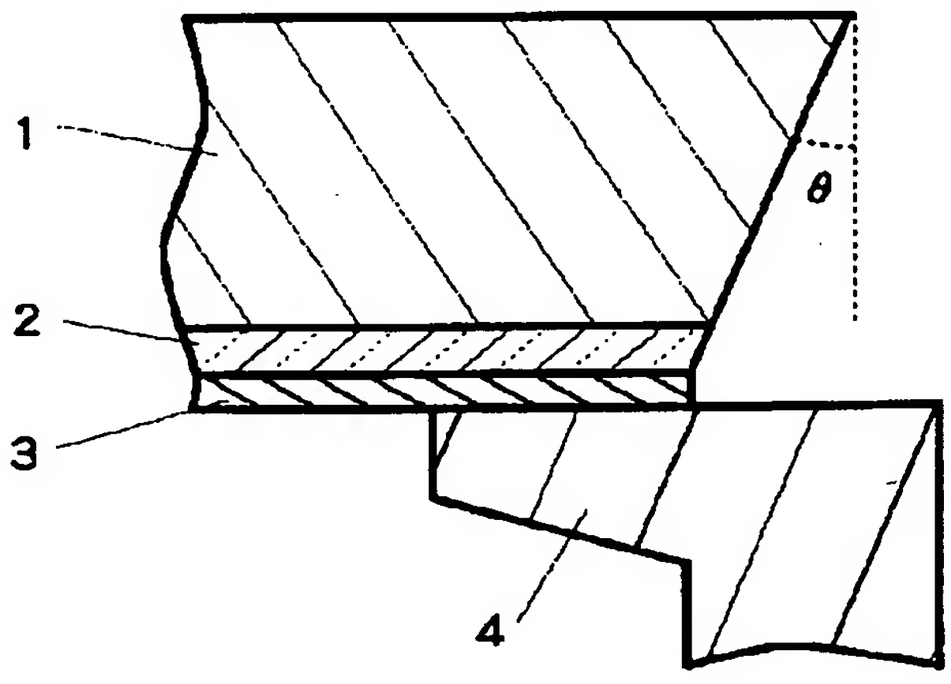
(54)【発明の名称】　青色発光ダイオード

(57)【要約】　（修正有）

【目的】　カップ等の反射板を必要とせず、窒化ガリウム系化合物半導体を利用した発光素子の側面から出る光を有効利用して、観測面側に取り出し、青色ＬＥＤの発光効率を向上させる。

【構成】　発光素子が少なくとも透光性基板１と該透光性基板に積層された窒化ガリウム系化合物半導体２とからなり、さらに該発光素子の透光性基板１を上面としてリードフレーム４上に載置し、発光素子全体を樹脂モールド５で封止してなる青色発光ダイオードにおいて、前記発光素子の側面が、透光性基板上面から鉛直方向に向かって、鋭角θで切断されていることを特徴とする。



【特許請求の範囲】
【請求項１】　発光素子が少なくとも透光性基板と該透光性基板に積層された窒化ガリウム系化合物半導体とからなり、さらに該発光素子の透光性基板を上面としてリードフレーム上に載置し、発光素子全体を樹脂モールドで封止してなる青色発光ダイオードにおいて、
前記発光素子の側面が、透光性基板上面の鉛直方向より、鋭角θで切断されていることを特徴とする青色発光ダイオード。
【請求項２】　前記鋭角θは、前記透光性基板の屈折率をｎ1、前記樹脂モールドの屈折率をｎ2とすると、$\theta \geqq sin^{-1}(n2/n1)$の関係にあることを特徴とする請求項１に記載の青色発光ダイオード。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、透光性基板上に窒化ガリウム系化合物半導体が積層された発光素子を有する青色発光ダイオード（以下、青色ＬＥＤという。）に係り、特に該発光素子の細部の構造に関する。
【０００２】
【従来の技術】一般に、青色ＬＥＤの発光素子の材料として、ＧａＮ、ＩｎＧａＮ、ＧａＡｌＮ、ＩｎＡｌＧａＮ等の窒化ガリウム系化合物半導体が知られている。これら窒化ガリウム系化合物半導体を用いた発光素子を有する従来の青色ＬＥＤの構造を図２に示す。１は透光性基板、２は透光性基板１上に積層された窒化ガリウム系化合物半導体（以下、本明細書においては、１と２とを合わせて発光素子という。）３は窒化ガリウム系化合物半導体２上の適切な位置に設けられた電極、４は発光素子を載置するリードフレーム、５は発光素子全体を封止し、窒化ガリウム系化合物半導体２からの発光を集光する樹脂モールドである。透光性基板１の材料にはサファイア、酸化亜鉛、酸化マグネシウム等の酸化物系単結晶を使用することができ、一般的にはサファイアが用いられている。また樹脂モールド５には、エポキシ樹脂、ユリア樹脂等、耐候性に優れた透明樹脂が用いられる。この図に示すように、従来の青色ＬＥＤはそのほとんどが、発光素子の端面が垂直になるようにチップ状にカットされ、透光性基板１側が上面、即ち発光観測面となるようにしてリードフレームに載置された構造を有している。
【０００３】
【発明が解決しようとする課題】この構造の発光素子において、例えば透光性基板１をサファイアとした場合、サファイア基板１の厚さは通常数百μｍある。これに対し、窒化ガリウム系化合物半導体の厚さはせいぜい数μｍにしか過ぎず、窒化ガリウム系化合物半導体より放射される全青色発光のうち、サファイア基板１の側面に達する光は、全体の約１０～４０％である。しかも、封止樹脂をエポキシ樹脂とした場合、サファイアの屈折率を約３とし、エポキシの屈折率を約１．５とすると、サファイアとエポキシ樹脂との境界での臨界角は約３０°となり、側面に入射する３０°以下の光は、全てサファイア基板の側面から出て行ってしまい、有効利用されていない。
【０００４】ところで、リードフレームの形状をカップ状として、そのカップの底に発光素子を載置して、側面から出ていく光を、カップ側面で上部に反射させる方法もあるが、リードフレームをカップ形状にすると、透光性基板を上にして電極を下にするような構造の窒化ガリウム系化合物半導体発光素子、つまり透光性基板を利用した発光素子では、アッセンブリが生産技術上不可能である。そのため、従来の青色ＬＥＤは、そのほとんどが図２のような構造であり、この構造のＬＥＤはチップ側面より出ていく光を有効利用できず、高い順方向電圧のわりに、発光効率が低く、十分な輝度が得られないという問題があった。
【０００５】したがって本発明はこのような事情を鑑みて成されたものであり、カップ等の反射板を必要とせず、窒化ガリウム系化合物半導体を利用した発光素子の側面から出る光を有効利用して、観測面側に取り出し、青色ＬＥＤの発光効率を向上させることを目的とする。
【０００６】
【課題を解決するための手段】本発明の青色ＬＥＤは、発光素子が少なくとも透光性基板と該透光性基板に積層された窒化ガリウム系化合物半導体とからなり、さらに該発光素子の透光性基板を上面としてリードフレーム上に載置し、発光素子全体を樹脂モールドで封止してなる青色発光ダイオードにおいて、前記発光素子の側面が、透光性基板上面の鉛直方向より、鋭角θで切断されていることを特徴とするものである。
【０００７】鋭角θの角度は特に限定するものではないが、透光性基板の屈折率、樹脂モールドの屈折率によって適宜変更することができる。窒化ガリウム系化合物半導体の発光を全て透光性基板側（発光観測面側）に全反射させるためには、鋭角θは、透光性基板の屈折率をｎ1、前記樹脂モールドの屈折率をｎ2とした場合、$sin^{-1}(n2/n1)$以上の角度、即ち臨界角以上の角度で切断されていることが好ましい。なお、この式により、全ての青色発光を発光素子側面で全反射させる場合、樹脂モールドの材料の屈折率が基板の屈折率よりも小さいものを選択することはいうまでもない。
【０００８】また、発光素子の側面を斜めにカットするには、例えばダイシングを用いることができ、刃先が所望の角度に調整されているブレードを使用することによって切断可能である。
【０００９】
【作用】図４は、本発明の一実施例に係る青色ＬＥＤにおいて、側面が鋭角θで切断された発光素子の構造を示す図である。また図３は、側面が垂直に切断された従来

の発光素子の構造を示す図である。なおこれらの図は電極、リードフレームを省略して示している。図４に示すように、発光素子の側面を、透光性基板１の上面から、鋭角θで切断することにより、窒化ガリウム系化合物半導体より発する青色発光、特に発光素子側面近傍の青色発光を、透光性基板１で反射させて発光観測面に取り出し、有効利用することが可能となる。一方、前にも説明したように、図３に示す従来の発光素子は、透光性基板１内で全反射したり、発光素子の側面から出て行ってしまう光が圧倒的に多い。なお、この図４はθを臨界角以上としていないため、一部側面から出ていく光もあるが、θを前述の式に基づいて臨界角以上で切断することにより、全て観測面側に反射させることができるのは当然である。

【００１０】このように、発光素子の側面を鋭角に切断することにより、青色発光を多く観測面に反射させることができるため、青色発光ダイオードの発光出力を向上させることができる。また、窒化ガリウム系化合物半導体を有する発光素子は、他のＧａＡｓ、ＧａＰ、ＡｌＩｎＧａＰ等の材料を用いた発光素子と異なり、材料自体にへき開性を有していないため、斜めに切断しやすいという利点を有している。このため、窒化ガリウム系化合物半導体の発光素子の側面を斜めに切断して、その側面で青色発光を反射させることは非常に重要である。

【００１１】

【実施例】予めサファイア基板の上にｎ型ＧａＮとｐ型ＧａＮとを順に積層した２インチφのウエハーを用意し、ｐ型ＧａＮ層の一部をエッチングして、ｎ型ＧａＮ層を一部露出させる。次に、露出させたｎ型ＧａＮ層と、ｐ型ＧａＮとに所定の形状で電極を蒸着した後、サファイア基板に粘着テープを張り付ける。

【００１２】一方、ウエハーを斜めにカットするため、図５に示すように刃先の中心線に向かってそれぞれ両側に３０°の傾斜を設けたブレードを用意してダイシングソーにセットする。次に、前述のウエハーをテーブルに貼付し、ダイシングでｐ型ＧａＮ層側からＸ軸をカットした後、テーブルを９０°回転させ、今度はＹ軸をカットする。

【００１３】最後にウエハーをテーブルから剥し取り、チップ状に分離した後、チップをサファイア基板面が発光観測面になるようにして、リードフレームに取り付け、電極とリードフレームとを電気的に接続した後、エポキシ樹脂でレンズ状にモールドすることにより、本発明の青色ＬＥＤを得る。

【００１４】このようにして得た青色ＬＥＤは、順方向電圧５Ｖで、発光出力２０μＷを示した。一方、側面を垂直にカットしたチップよりなる従来の青色ＬＥＤは発光出力は１０μＷとほぼ半分しかなかった。

【００１５】

【発明の効果】以上説明したように、本発明の青色ＬＥＤはその発光素子の側面を斜めにカットしているために、窒化ガリウム系化合物半導体の発光を、その側面で反射させて透光性基板から有効に取り出すことができる。しかも従来のようにカップ状のリードフレームも必要とせず、生産性にも非常に優れている。

【図面の簡単な説明】

【図１】　本発明の青色ＬＥＤに係る発光素子の側面の構造を一部拡大して示す断面図。

【図２】　従来の青色ＬＥＤの構造を示す断面図。

【図３】　従来の発光素子の構造を示す断面図。

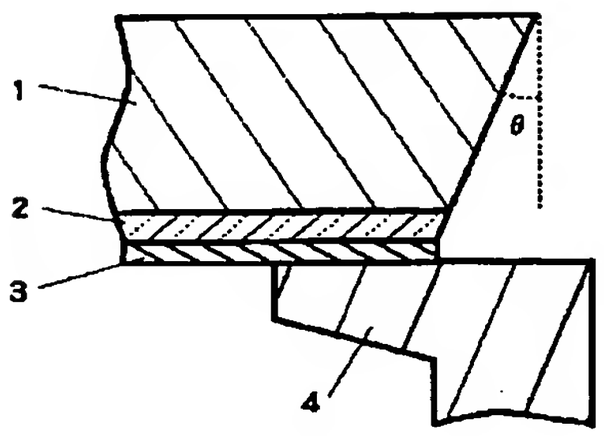
【図４】　本発明の一実施例に係る発光素子の構造を示す断面図。

【図５】　ダイシングソーのブレードの刃先角を示す断面図。

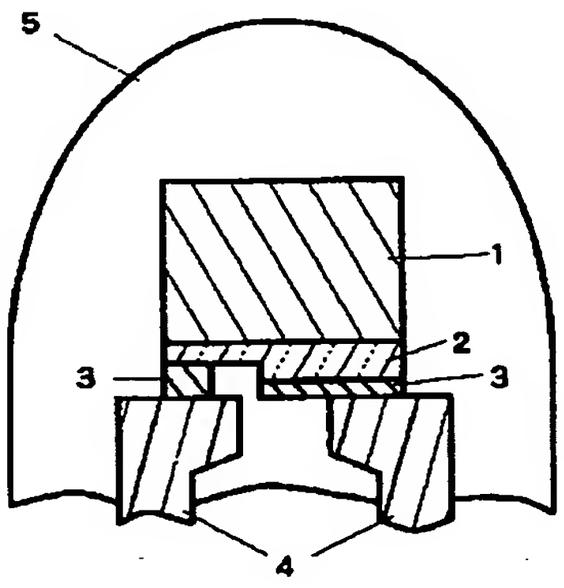
【符号の説明】

１・・・・・・透光性基板
２・・・・・・窒化ガリウム系化合物半導体
３・・・・・・電極
４・・・・・・リードフレーム
５・・・・・・樹脂モールド

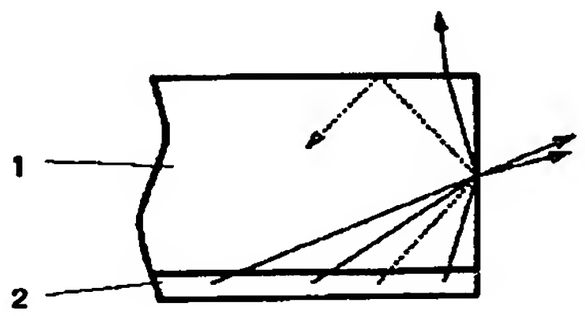
【図１】



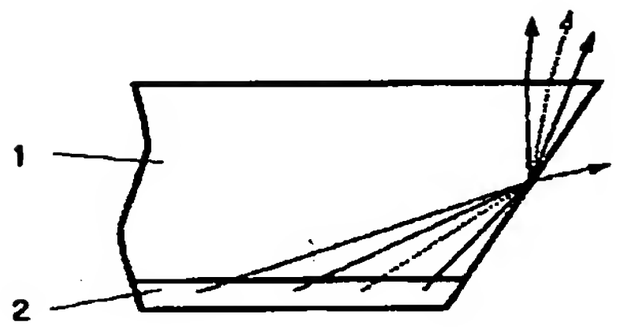
【図２】



【図３】



【図４】



【図５】